High-order Modulation scheme based on combinational QPSK accelerators for HSPA Evolution in UE

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Abstract— the UMTS Channel Unit Processor for 3GPP Base Station introduced earlier in its early version is an advanced 3G BTS baseband processing ASIC accelerator. Originally, this ASIC was targeted for WCDMA baseband function processing. With the deep study of its design flexibility in SW programming and HW architecture, the accelerator can be extended to support 3GPP Release 6 HSDPA functions. While with the progress in 3GPP standardization and evolution [4], there is a further need to either develop new generation of ASIC accelerators to accommodate the evolutional movement with high cost of R&D expenses, or in parallel to make re-use of this ASIC accelerator’s low cost to deploy new structures with adequate SW changes and appropriate HW combinations for the existing ASIC circuitries. This has been proven possible to support 3GPP Release 7 EDCH QPSK scheme [2] on this flexible ASIC accelerator. Furthermore, the long term HSPA evolution requires supporting much higher order modulation schemes with spectral efficiencies in both downlink and uplink, such as with multiple antennas and 64QAM, the system should accomplish peak DL Tput 21 Mbps, 42 Mbps, 84 Mbps or even higher. Based upon this technical background, this paper continues looking into the Channel Unit Processor ASIC accelerator and uses the combinations of the basic QPSK structures to fully implement all the possible modulation schemes from BPSK, rotated QPSK, 4PAM, 16QAM, and 64QAM. At the end the paper gives out a general form of the combinational implementation for the higher order QAM (HOM) schemes.

Index Terms—ASIC, HOM, HSPA, QPSK.

I. INTRODUCTION

The UMTS Channel Unit Processor for 3GPP Base Station introduced earlier in [1] [2] is an advanced 3G BTS baseband processing ASIC accelerator. Originally, this BB ASIC was targeted for WCDMA baseband function processing. With the deep study of its design flexibility in SW programming and HW architecture, the accelerator can be extended to support 3GPP Release 6 HSDPA functions. While with the progress in 3GPP standardization and evolution [4], there is a further need to either develop new generation of ASIC accelerators to accommodate the evolutional movement with high cost of R&D expenses, or in parallel to make re-use of this ASIC accelerator’s low cost to deploy new structures with adequate SW changes and appropriate HW combinations for the existing ASIC circuitries. This has been proven possible to support 3GPP Release 7 EDCH QPSK scheme [2] on this flexible ASIC accelerator. Furthermore, the long term HSPA evolution requires supporting much higher order modulation schemes with spectral efficiencies in both downlink and uplink, such as with multiple antennas and 64QAM, the system should accomplish peak DL Tput 21 Mbps, 42 Mbps, 84 Mbps or even higher. Based upon this technical background, this paper continues looking into the Channel Unit Processor ASIC accelerator and uses the combinations of the basic QPSK structures to fully implement all the possible modulation schemes from BPSK, rotated QPSK, 4PAM, 16QAM, and 64QAM and even higher order QAM (HOM) modulators. The paper will demonstrate that it is possible to generate a BPSK signal using half of the QPSK transmitter with I or Q branch programmed to “0”, and it is possible to generate a 16-QAM signal using two QPSK transmitters for HSDPA and EDCH, and it is also possible to generate a 64-QAM signal using three QPSK transmitters for the evolved HSDPA and EDCH as well. All the work can be done in SW [3] configuration without the ASIC accelerator’s upgrade. Currently the deployed HOM modulators are targeted for implementation in the UE emulator equipment, which supports the development of HSPA BTS equipments being used in North America and worldwide.

II. HIGH ORDER MODULATION (HOM) SCHEME FOR HSDPA AND EDCH

The HSPA evolution in 3GPP Release 7, 8, 9 and so on deploys high order modulation (HOM) schemes to obtain high data rate and high frequency spectrum efficiency. The
Modulation scheme shown in cells in Figure 1 can be adaptively changed according to the distance from Mobile Station to the Base Station with the link adaptation Algorithm in the Scheduler. In Release 6, it has also been proven by simulations that the HSDPA Tput can reach 14.4Mbps. Using 64QAM and MIMO, the MAX DL Tput for HSDPA can reach 21.6 Mbps, etc.

With the UMTS Channel Unit Processor [1] [2] which has 8 general-purpose QPSK transmitter ASIC accelerators, even without a HW update, the paper will show us step by step that we can find a way to generate a BPSK signal using half of the QPSK transmitter by setting I or Q branch to be “0”, we can also find a way to generate a 16-QAM signal using two QPSK transmitter accelerators, and a 64-QAM signal using three QPSK transmitters, and so on for more higher order modulation (HOM) schemes.

III. BPSK ASIC ACCELERATOR

As seen in Figure 2 below, a QPSK modulator can be used for BPSK by ignoring the I branch. That is to say, one QPSK transmitter can transmit two BPSK symbols modulated in different branches, such as one is in the I branch, the other is in Q. With this method, EDCH modulation can be supported.

IV. QPSK ASIC ACCELERATOR

Basic HSPA modulation ASIC Tx block and constellation can be shown as Figure 3. This is actually the fundamental design in the UMTS Channel Unit Processor for WCDMA. We should note that before the signal inputting to the QPSK accelerator, there is a Binary code to Gray code conversion function block ahead of the QPSK modulator.

\[
g_n = b_n + 1 \times OR \ b_n \;
\]

\[
g_N = b_N \times OR \ 0 = b_N\ ;\ for\ the\ MSB
\]

We should keep this in mind as it is the original design [1][2], and all of our changes and improvements introduced in this paper start from this basic QPSK ASIC.

V. A ROTATED QPSK ASIC ACCELERATOR

According to research reports in [5][6], a rotated constellation can obtain modulation diversity by rotating certain angles and using component interleaving. For example, a usual QPSK constellation (A,B) becomes a new rotated

\[
\begin{bmatrix}
X \\
Y
\end{bmatrix} = R \begin{bmatrix}
A \\
B
\end{bmatrix} = \begin{bmatrix}
\cos \theta & \sin \theta \\
-\sin \theta & \cos \theta
\end{bmatrix} \begin{bmatrix}
A \\
B
\end{bmatrix}
\]

Let’s define \( \theta = \pi/4 - \alpha \)
\[\alpha = \arctan (A/B),\]

Then by adjusting the \( \theta \) with DSP SW programming, an optimum modulation diversity can be obtained to minimize bit error rate (BER) that is in accordance with the research results reported in [5][6]. In the implementation of the rotated modulation scheme, we need to use 2 basic ASIC QPSK Tx Accelerators as described in Section IV, the reconstructed rotated QPSK constellation scheme is shown in Figure 4.

VI. 4-PAM ASIC ACCELERATOR

Also, 4-PAM, a new modulation scheme in EDCH Release
can be realized by two QPSK modulator accelerators. Transmitter 1 has amplitude 2A, and transmitter 2 has amplitude A, as illustrated by Figure 5. The transmitter signal can be represented by \( Tx = A \times (2 \times I_0 + I_1) \), where \( A = 0.4472 \) is the Tx Power level scaling factor for QPSK modulators: 1,2.

**VII. 16-QAM ASIC ACCELERATOR**

For 16-QAM, each four consecutive bits: \( b_0, b_1, b_2, b_3 \) can generate one 16-QAM symbol. Figure 6 shows how to generate one 16-QAM symbol with two QPSK symbols. And the generation of the 16-QAM symbols with Gray Coded bits by using the two (QPSK) transmitters is as Figure 7 shown.

Let us suppose the Transmitter 1 has amplitude 2A, the symbols fed to transmitter 1 are: \( I_1 = b_0 \oplus b_2 \), \( Q_1 = b_1 \oplus b_3 \).

Then the symbols fed to transmitter 2 are:

\[
I_2 = b_0 \oplus b_1 = b_0 \oplus b_2, \quad Q_2 = b_1 \oplus b_3 = b_1 \oplus b_3.
\]

Table-1 shows the logic table of the implementation of 16-QAM using the UMTS Channel Element basic QPSK accelerator. In Table-1, the I and Q represent the signals on the real and imaginary branches before spreading and scrambling.

<table>
<thead>
<tr>
<th>( b_0b_1b_2b_3 )</th>
<th>I branch</th>
<th>Q branch</th>
</tr>
</thead>
<tbody>
<tr>
<td>0000</td>
<td>0.4472</td>
<td>0.4472</td>
</tr>
<tr>
<td>0001</td>
<td>0.4472</td>
<td>1.3416</td>
</tr>
<tr>
<td>0010</td>
<td>1.3416</td>
<td>0.4472</td>
</tr>
<tr>
<td>0011</td>
<td>1.3416</td>
<td>1.3416</td>
</tr>
<tr>
<td>0100</td>
<td>0.4472</td>
<td>-0.4472</td>
</tr>
<tr>
<td>0101</td>
<td>0.4472</td>
<td>-1.3416</td>
</tr>
<tr>
<td>0110</td>
<td>1.3416</td>
<td>-0.4472</td>
</tr>
<tr>
<td>0111</td>
<td>1.3416</td>
<td>-1.3416</td>
</tr>
<tr>
<td>1000</td>
<td>-0.4472</td>
<td>0.4472</td>
</tr>
<tr>
<td>1001</td>
<td>-0.4472</td>
<td>1.3416</td>
</tr>
<tr>
<td>1010</td>
<td>-1.3416</td>
<td>0.4472</td>
</tr>
<tr>
<td>1011</td>
<td>-1.3416</td>
<td>1.3416</td>
</tr>
<tr>
<td>1100</td>
<td>-0.4472</td>
<td>-0.4472</td>
</tr>
<tr>
<td>1101</td>
<td>-0.4472</td>
<td>-1.3416</td>
</tr>
<tr>
<td>1110</td>
<td>-1.3416</td>
<td>-0.4472</td>
</tr>
<tr>
<td>1111</td>
<td>-1.3416</td>
<td>-1.3416</td>
</tr>
</tbody>
</table>

The transmitter signal can be represented by

\[
Tx = A \times (2xI0+I1 + j (2xQ0+Q1) \times Cch x Sul ),
\]

where \( A = 0.3162 \) is the Tx Power level scaling factor for QPSK modulators: 1,2.

More generally, using two QPSK modulators with different amplitudes we can realize multi-resolution 16-QAM modulation that can be used in MBMS for MIMO UTRA LTE system [7]. Suppose that the transmitter 1 has amplitude M, and transmitter 2 has amplitude N, as illustrated by Figure 8, then the transmitter signal can be represented by

\[
Tx = A \times ( (M \times I_0 + I_1) \times Cch x Sul ) \]

Figure 6. Using Two QPSK to construct a 16QAM

Figure 7. Using 2 ASIC QPSK accelerators to implement a 16-QAM

Figure 8. Multi-resolution 16QAM modulation
x I0+N x I1) + j (M x Q0 + N x Q1) x Cch x Sul ],
A = \frac{1}{\sqrt{(M - N)^2 + (M + N)^2}}
which is the Tx Power level scaling factor for QPSK modulators: 1, 2.

VIII. 64 QAM ASIC ACCELERATOR

64-QAM high order modulation can be constructed by 3 QPSK modulators, which can be seen in Figure 9. The transmitter signal can be represented by:

\[ Tx = A \left( (4 x I0 + 2 x I1 + I2) + j (4 x Q0 + 2 x Q1 + Q2) \right) x Cch x Sul \]

Here A = 0.1543, which is the Tx Power level scaling factor for QPSK modulators: 1, 2, 3.

IX. GENERAL \(2^{2M}\) QAM HOM ASIC ACCELERATOR

With the similar procedure as demonstrated from section III to VIII, we can construct much higher order QAM modulation schemes, such as 256-QAM, etc. That is to say we can construct the HOM constellations in a systematic way as we construct in HW and program in SW for 16-QAM and 64-QAM with only the basic ASIC Tx accelerator blocks. As far as the 3GPP is defined, there is still no higher modulation scheme than 64QAM at the moment for the HSPA evolution either on BTS side or on UE side, but much higher order modulation is always an option item in communication systems. In regard to this aspect, it is still worthwhile to study general form higher order modulation (HOM) schemes and give their general representation. Here for the general \(2^{2M}\) QAM scheme, the Tx signal can actually be represented by a general form:

\[ T_x = A \cdot \sum_{m=0}^{M-1} \left( 2^m \left( I_{M-m-1} + j Q_{M-m-1} \right) \right) \]

Now we stand at for studying the basic QPSK ASIC accelerator and applying it to higher order modulations. As can be seen from the whole paper, all the HOM engines can be realized flexibly in SW without further ASIC fabrication or upgrade. The BPSK signal can be implemented by using half of the QPSK transmitter with I or Q branch programmed to “0”. A 16-QAM signal can be implemented by using two QPSK transmitters for HSDPA and EDCH. A 64-QAM signal can be implemented by using three QPSK transmitters for the evolved HSDPA and EDCH, and so on. All the work can be done in SW configuration and currently the deployed HOM modulators have been implemented in the 3G MTE emulators to support the development of HSPA BTS equipments being used extensively in 3G networks in North America and worldwide.

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